CLAIMS

I claim:

1. A subranging analog-to-digital converter (ADC), comprising:

a first integrating sample-and-hold circuit configured to sample an input voltage by charging a first capacitor through a first current switch;

a first stage having a coarse-quantizing ADC configured to digitize a voltage on the first capacitor to provide a coarsely-digitized output and a DAC configured to convert the coarsely-digitized output into an analog voltage;

a second integrating sample-and-hold circuit configured to sample the input voltage by charging a second capacitor through a second current switch; and

a second stage configured to receive charge from the charged second capacitor and the analog voltage to provide a voltage difference between the sampled input voltage and the analog voltage, the second stage including a fine-quantizing ADC configured to convert the voltage difference to provide a finely-digitized output.

2. The subranging ADC of claim 1, wherein the second stage is configured to provide the voltage difference by comprising a third capacitor having a first terminal and an opposing second terminal, wherein the subranging ADC is configured to couple the first terminal to the charged second capacitor and to couple the opposing second terminal to the complement of the analog voltage such that the first terminal is charged to the voltage difference.

3. The subranging ADC of claim 1, wherein the first integrating sample-and-hold circuit includes a differential pair of transistors configured as a current switch.

4. The subranging ADC of claim 3, further comprising a first transconductance circuit operable to convert the input voltage into the current that is switched by the differential pair of transistors.

5. The subranging ADC of claim 4, wherein the second integrating sample-and-hold circuit includes a differential pair of transistors configured as a current switch.

6. The subranging ADC of claim 5, further comprising a second transconductance circuit operable to convert the input voltage into the current that is switched by the differential pair of transistors in the second integrating sample-and-hold circuit.

7. The subranging ADC of claim 6, wherein a transconductance constant implemented by the second transconductance circuit is greater than a transconductance constant implemented by the first transconductance circuit.

8. The subranging ADC of claim 6, wherein the differential pairs of transistors comprise bipolar transistors.

9. The subranging ADC of claim 2, wherein the second stage further includes a buffer amplifier operable to buffer the voltage difference from the fine-quantizing ADC.

10. The subranging ADC of claim 9, further comprising combining logic operable to combine the finely-digitized output and the coarsely-digitized output to provide a digitized output corresponding to the sampled input voltage.

11. The subranging ADC of claim 10, wherein the subranging ADC is configured to sample the input voltage in a double-ended fashion.

12. The subranging ADC of claim 10, wherein the subranging ADC is configured to sample the input voltage in a single-ended fashion.

13. The subranging ADC of claim 10, further comprising a reset circuit operable to reset the second capacitor while transferring the integrated charge on the second capacitor to the first terminal of the third capacitor.

14. A method of digitizing an input voltage, comprising:

converting an input voltage to a first current;

closing a first current switch to couple the first current to a first capacitor to charge the first capacitor;

converting the input voltage to a second current;

closing a second current switch to couple the second current to a second capacitor to charge the second capacitor;

coarsely-quantizing a voltage on the charged first capacitor to provide a coarsely-

digitized output;

converting the coarsely-digitized output into an analog voltage;

transferring the charge from the charged second capacitor to a first terminal of a third capacitor and shifting the voltage of an opposing second terminal of the third capacitor to the negative of the analog voltage to produce a residual voltage at the first terminal of the third capacitor representing a difference between the voltage on the charged first capacitor and the analog voltage; and

finely-quantizing the residual voltage to provide a finely-digitized output.

15. The method of claim 14, further comprising combining the finely-digitized output and the coarsely-digitized output to form a digitized output.

16. A subranging ADC, comprising:

a first integrating sample-and-hold circuit configured to sample an input voltage by charging a first capacitor, the first capacitor being charged by a coupling a first current proportional to the input voltage through at least one differential pair of transistors configured as a switch for the first current;

a coarsely-quantizing ADC configured to convert a voltage on the charged first capacitor to a coarsely-digitized output;

a DAC configured to convert the coarsely-digitized output to an analog voltage;

means for determining a residual voltage equaling the difference between the analog voltage and the voltage on the charged first capacitor; and

a finely-quantizing ADC configured to convert the residual voltage into a finely-

quantized output.

17. The subranging ADC of claim 17, further comprising:

a second integrating sample-and-hold circuit configured to sample an input voltage by charging a second capacitor, the second capacitor being charged by a coupling a second current proportional to the input voltage through at least one differential pair of transistors configured as a switch for the second current; and

wherein the means includes a third capacitor configured to determine the residual voltage by receiving the charge from the charged second capacitor at a first terminal and by receiving a shift in voltage equal to the complement of the analog voltage at an opposing second terminal.

18. The subranging ADC of claim 17, further comprising:

a first transconductance circuit operable to convert the input voltage into the first current; and

a second transconductance circuit operable to convert the input voltage into the second current.

19. The subranging ADC of claim 18, wherein the input voltage is a differential input voltage.

20. The subranging ADC of claim 19, further comprising:

resetting means for resetting the second capacitor, wherein the resetting means is

configured to charge the third capacitor and shift the voltage at one terminal of the third capacitor so as to produce the residual voltage on an opposing terminal of the third capacitor while resetting the second capacitor.